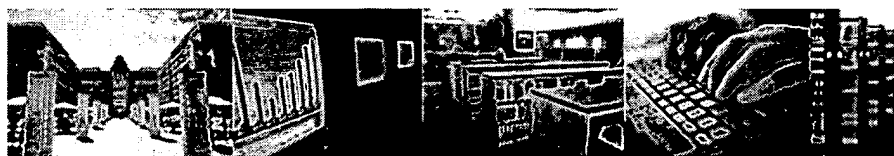



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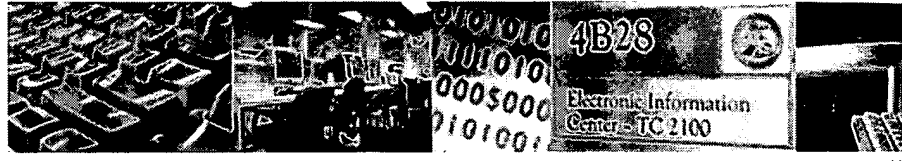
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Joachim Altmeyer, Stefan Ohnsorge, Bernd Schürmann

November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**Full text available: [pdf\(851.80 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The reuse of well-tested and optimized design objects is an important aspect for decreasing design times, increasing design quality, and improving the predictability of designs. Reuse spans from the selecting cells from a library up to adapting already designed objects. In this paper, we present a new model for reusing design objects in CAD frameworks. Based on experiences in other disciplines, mainly in software engineering and case-based reasoning, we developed a feature-based m ...

2 [On modeling top-down VLSI design](#)

Bernd Schürmann, Joachim Altmeyer, Martin Schütze

November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**Full text available: [pdf\(908.16 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

We present an improved data model that reflects the whole VLSI design process including bottom-up and top-down design phases. The kernel of the model is a static version concept that describes the convergence of a design. The design history which makes the semantics of most other version concepts, is modeled explicitly by additional object classes (entities types) but not by the version graph itself. Top-down steps are modeled by splitting a design object into requirements and realizations. ...

3 [Generating ECAD framework code from abstract models](#)

Joachim Altmeyer, Bernd Schürmann, Martin Schütze

January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation**Full text available: [pdf\(60.96 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

4 [Representing reductions of NP-complete problems in logical frameworks: a case study](#)

Carsten Schürmann, Jatin Shah

August 2003 **Proceedings of the 2003 workshop on Mechanized reasoning about languages with variable binding**Full text available: [pdf\(206.80 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Under the widely believed conjecture $P \neq NP$, NP-complete problems cannot be solved exactly using efficient polynomial time algorithms. Furthermore, any instance of a NP-complete problem can be converted to an instance of another problem in NP in polynomial time. Thus, identifying NP-complete problems is very important in algorithm design and can help computer scientists and engineers redirect their efforts towards finding approximate solutions to these problems. As a first step towards a digita ...

Keywords: NP-complete problems, linear logic, logical frameworks

5 Three-phase chip planning — an improved top-down chip planning strategy

Bernd Schürmann, Joachim Altmeyer, Gerhard Zimmermann

November 1992 **Proceedings of the 1992 IEEE/ACM international conference on Computer-aided design**

Full text available:  [pdf\(980.54 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

6 Modeling design tasks and tools: the link between product and flow model

Bernd Schürmann, Joachim Altmeyer

June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Full text available:  [pdf\(73.26 KB\)](#)  Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)
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The important step towards a comprehensive CAD framework is the development of a suitable, completed design model on which the design system's components are based. To date, we generally find "island" solutions for different aspects as data and process management, but in future, we need more and more integrated solutions. Only the integration gives us the traceability we need for design planning, to generate parts of the design tool's code automatically, etc. This paper describes how a suitable Design Ta ...

7 The effect of pin constraints on layout area

B. Schurmann, J. Altmeyer

March 1995 **Proceedings of the 1995 European conference on Design and Test**

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We present an improved area estimation model that considers the large influence of pin positions on the layout area. The estimation method is based on the shape function approach described by Zimmermann (1988). A cell is abstracted at all hierarchy levels by discrete shape functions describing its area with respect to its shape. The internal wiring area is estimated by a simple but proper statistical model. Although the basic approach is one of the most accurate hierarchical area estimation mode ...

Keywords: hierarchical area estimation model, integrated circuit layout, integrated circuit modelling, internal wiring, layout area, pin positions, shape functions, statistical model, top-down design

8 Business Applications: GAN, a system for generating and analyzing activity networks

A. Schurmann

October 1968 **Communications of the ACM**, Volume 11 Issue 10

Full text available:  [pdf\(606.33 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

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GAN, a system for generating activity networks, is designed to save time in the preparation of activity networks and to deal conveniently with network programs. A defining description of a programming language designed for generating activity network from a set of standard networks is presented. Also, a general idea of a language for performing calculations on activity networks (scheduling activity networks) is given.

Keywords: activity network, activity network analysis, management project, network assembler, network calculation, network generator, network program, standard network

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